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EXAMINER	
WALTER, CRAIG E	
ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,886	JOHNSON, BRIAN P.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-42 are pending in the Application.

Claims 1, 7, 10-11, 13-14, 19, 22-23, 25, 26, 31, 33, 39, 42 have been amended.

Claims 1-42 are rejected.

Response to Amendment

2. Applicant's amendments and arguments filed on 27 April 2006 in response to the office action mailed on 13 March 2006 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Drawings

3. The drawings (Figures 1 and 2) were received on 27 April 2006. These drawings are deemed acceptable.

4. The drawings are objected to because of the following reasons:

Element 316 in Figure 3 should be rewritten to accurately reflect this step in view of the description provided in paragraph 0029 of the specification. More specifically, paragraph 0029, lines 3-4 of the original specification recite element 316 as including "the BIOS determin[ing] if the memory configuration data as provided in the CMOS is valid", yet the original drawing recites "has the information file been previously accessed" for this element. Examiner respectively requests Applicant clarify which step (checking the validity as per the specification, or checking if the file has been accessed

as per the drawings) most accurately defines what is believed to be the claimed invention.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 33-42 are rejected under 35 U.S.C. 101 because the claimed invention is not limited to statutory subject matter as the machine-readable medium recited in these claims recite both statutory subject matter (i.e. EEPROM) and non-statutory subject matter (i.e. carrier waves). Please refer to paragraph 0036 of the specification. More specifically, carrier waves or signals *per se* do not fall into one of the four statutory categories of invention as defined by section 101 of the Code. Please refer to the discussion presented *infra* (under paragraph heading 26) for more detail as to the justification of maintaining this rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Nizar et al. (US Patent 6,378,056 B2), hereinafter Nizar.

As for claims 1, 33 Nizar teaches a method and machine-readable medium comprising:

a memory unit (Fig. 1, element 104); and

a first unit (Fig. 5, element 500 – memory controller, or MCH) to access a first unit of data from a non-volatile device of the memory unit (referring to Fig. 5, and col. 13, line 52 through col. 14, line 8 – information stored in the module's SPD (which is non-volatile memory) is read by the MCH via the serial interface in the ICH (element 505)), the first unit of data including a characteristic of the memory unit (the SPD stores configuration data on the RDRAM (Fig. 5, elements 573, 574, etc. and the RIMM – 570) – col. 14, lines 26-37),

and the first unit to access, based on the content of the first unit of data, a second unit of data stored in a separate storage device from the memory unit to retrieve additional characteristics of the memory unit (col. 14, lines 26-37 – SPD configuration data is read from the RDRAM devices. The memory controller registers are then programmed with values from the SPD so that the controller can uniquely access each RDRAM device. Referring to Fig 5, the memory controller (500) comprises initialization registers (515) used to store information related to each of the RDRAM device (col. 13, lines 21-43)). Once the initialization process begins, data related to the RDRAMs is read from the SPD. This information is then used to populate the controller's registers (i.e. separate

storage device) with characteristic data on each RDRAM (col. 14, lines 26-37). The system must now use the information in the controller's registers in order to appropriately access the RDRAM devices (col. 14, lines 38-52). In summary, the system accesses the SPD in order to obtain configuration data, which in turn is used to program registers of the memory controller. Once the system is initialized, the characteristic data must be accessed from the controller registers in order to extract the appropriate information to access the RDRAM devices. The registers of the controller are separate from the SPD non-volatile memory location.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nizar (US Patent 6,378,056 B2) in view of Wilcox et al. (US PG Publication 2003/0061458 A1), hereinafter Wilcox.

As for claim 25, though Nizar teaches all of the elements of claim 1 (as described above), he fails to teach his system including either a graphics controller, or cd-rom drive as recited in claim 25.

Wilcox however teaches a memory control with lookahead power management system, which includes a graphics controller coupled to a memory controller (Fig. 1). Additionally Wilcox teaches his system as utilizing a cd-rom drive (paragraph 0022, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Wilcox's system of power management. By doing so, Nizar could benefit by further including a means of reducing power consumption of DRAM devices, by placing them into low power states while not in use, as taught by Wilcox (paragraph 0003 – all lines).

8. Claims 2 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Nizar (US Patent 6,378,056 B2) as applied to claims 1, 13 and 33 above, and in further view of Manowitz (US PG Publication 2001/0039603 A1).

As for claims 2, 14, and 34, though Nizar teaches accessing a second unit of data, he fails to teach accessing one from a group comprising a hard disk, floppy disk, CD-ROM or a separate computer interconnected via a network.

Manowitz however teaches a system which stores solid state memory cards in a device bay over a network (referring to Fig. 3 – element 212). It is worthy to note that the bay it self is just one of a plurality of elements including a separate computer (Fig. 2, PC element 206) of the network – (paragraphs 0017 and 0018, all lines). Therefore the device bay (Fig. 2, element 212) can be accessed via the computer through the network.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Manowitz's networked device bay storage for his own to access his own memory modules. By doing so, Nizar would benefit by having a system to dynamically change the memory capacity of his system over a network by simply adding or removing modules from the bay (paragraph 0015, all lines). Nizar would also benefit by using the IEEE-1394 interface, which prevents data loss during live connection/disconnection of the memory (paragraph 0002, all lines).

9. Claims 3-4, 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2) and Manowitz (US PG Publication 2001/0039603 A1) as applied to clams 2, 14, and 34 above, and in further view of Williams et al. (US Patent 6,507,530 B1), hereinafter Williams.

As for claims 3-4 and 35-36, though the combined teachings of Nizar and Manowitz fail to teach the second unit of data as a memory module information file. Williams however teaches a weighted throttling mechanism with rank based throttling for a memory system wherein command information (i.e. memory module information file) is obtained from a plurality of device ranks. The controller uses the command information to generate a power weight value based on this information. The controller compares the stored power count of the ranks to a threshold to determine if the controller is to throttle the memory (see abstract). It is worthy to note that power values must be stored while the throttling logic (Fig. 1) increments before the comparison can be performed (Williams explicitly discloses the use of registers for storage). In other words, a

subunit (i.e. power count) is stored to make the determination. Col. 4, lines 4-16 further illustrates storing the power value.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Williams's throttling based mechanism for a memory system in his own memory system. By doing so, Nizar would benefit by having a means of throttling his memory units, hence reducing the likelihood of thermal overstress of the memory, as taught by Williams, col. 1, lines 33-38.

10. Claims 5-6, 9-10, 37-38 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2) and Manowitz (US PG Publication 2001/0039603 A1) and Williams (US Patent 6,507,530 B1) as applied to claims 4, 16 and 36 above, and in further view Koga (US PG Publication 2001/0026487 A1).

As for claims 5, 10, 37, and 42 the combined teachings of Nizar, Manowitz, and Williams fail to teach the information stored in his memory modules as including the either operating frequencies, or the manufacturer of the memories.

Koga however teaches storing the operating frequencies and manufacturer of the memories in the memories themselves (paragraph 0031, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to include Koga's apparatus into his own memory module system. By doing so, Nizar would benefit by having a memory module system

that achieves a higher operation speed by utilizing both on-board type memory modules, and slot-type memory modules to reduce the need to increase the installation area as taught by Koga (paragraph 0012, all lines).

As for claims 6 and 38, Nizar teaches accessing the second unit in response to initial booting of the computer system (Fig. 6 describes the process starting with system restart).

As for claims 9 and 41, Nizar teaches the information as being accessed by the BIOS (col. 3, lines 58-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to include Koga's apparatus into his own memory module system. By doing so, Nizar would benefit by having a memory module system that achieves a higher operation speed by utilizing both on-board type memory modules, and slot-type memory modules to reduce the need to increase the installation area as taught by Koga (paragraph 0012, all lines).

11. Claims 7-8 and 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2), Manowitz (US PG Publication 2001/0039603 A1), Williams (US Patent 6,507,530 B1), Koga (US PG Publication 2001/0026487 A1) as applied to claims 5, 17, and 37 above, and in further view Azevedo et al. (US PG Publication 2003/0221072 A1), hereinafter Azevedo.

As for claim 7 and 39, Nizar fails to teach the second unit of data as being accessed in response to a change in the memory controller register.

Azevedo however teaches an apparatus for increasing processor performance in a computing system, which includes a memory controller which contains a dirty bit. The dirty bit indicates if data in the memory has been changed. If the dirty bit is changed to indicate the line is dirty, the controller will access the memory by flushing the cache (paragraph 0065, all lines). In other words, once a change occurs to this bit (i.e. register), the memory will be accessed.

As for claims 8 and 40, again Nizar fails to teach the second unit of data as being accessed in response to an indication that the module information file have not be accessed.

Azevedo however teaches requesting data depending on the validity of the data and the tag portion of the address. The memory can be accessed if it is determined that an exact comparison occurs (data is valid as it has not been accessed since newly written – paragraph 0061, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Azevedo's apparatus into his own memory system. By doing so, Nizar could improve his processor's response to memory requests as suggested by Azevedo in paragraph 0020, all lines.

12. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2), Manowitz (US PG Publication 2001/0039603 A1), Williams (US Patent 6,507,530 B1), Koga (US PG Publication 2001/0026487 A1) as applied to claims 10 and 21 above, and in further view Haas et al. (US PG Publication 2005/0050266 A1), hereinafter Haas.

As for claim 11 Nizar fails to teach parsing the information file as recited in these claims.

Haas however teaches a method for storing data independent memories, which includes parsing data into data segments, and storing those segments into a non-volatile memory (paragraph 0020, lines 1-10). Examples of non-volatile memory are provided in paragraph 0029, lines 1-13.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include parsing of the data into his own memory system. By doing so, Nizar would have a means of providing redundancy for data in his system, in case a memory failure occurs as taught by Haas (paragraph 0002, all lines).

13. As for claim 12, though Williams teaches his information file as supporting DRAM, he fails to teach support SRAM, or FLASH memory. However it would have been obvious to a person of ordinary skill in the art at the time of the invention to further include these two well-known memories. One of ordinary skill in the art would have been motivated to do so, to improve the access time to the memory.

Examiner takes Official Notice (see MPEP section 2144.03) that these two memories were well known when the invention was made. The Applicant is entitled to traverse any/all official notice taken in this action according to MPEP section 2144.03. However, MPEP section 2144.03 further states "See also In re Boon, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice)." Specifically, In re Boon, 169 USPQ

231, 234 states "as we held in Ahlert, an applicant must be given the opportunity to challenge either the correctness of the fact asserted or the notoriety or repute of the reference cited in support of the assertion. We did not mean to imply by this statement that a bald challenge, with nothing more, would be all that was needed". Further note that 37 CFR section 671(c)(3) states "Judicial notice means official notice". Thus, a traversal by the Applicant that is merely "a bald challenge, with nothing more" will be given very little weight.

Since Applicant has failed to traverse Examiner's assertion that SRAM and FLASH memories are well-known in art in response to the previous correspondence, these memories are taken to be admitted prior-art per MPEP § 2144.03 (paragraph C).

14. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2) and Wilcox (US PG Publication 2003/0061458 A1) as applied to claim 26 above, and in further view Manowitz (US PG Publication 2001/0039603 A1).

As for claim 26, though Nizar teaches accessing a second unit of data, he fails to teach accessing one from a group comprising a hard disk, floppy disk, CD-ROM or a separate computer interconnected via a network.

Manowitz however teaches a system which stores solid state memory cards in a device bay over a network (referring to Fig. 3 – element 212). It is worthy to note that the bay it self is just one of a plurality of elements including a separate computer (Fig. 2, PC element 206) of the network – (paragraphs 0017 and 0018, all lines). Therefore the

device bay (Fig. 2, element 212) can be accessed via the computer through the network.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Manowitz's networked device bay storage for his own to access his own memory modules. By doing so, Nizar would benefit by having a system to dynamically change the memory capacity of his system over a network by simply adding or removing modules from the bay (paragraph 0015, all lines). Nizar would also benefit by using the IEEE-1394 interface, which prevents data loss during live connection/disconnection of the memory (paragraph 0002, all lines).

15. Claims 27-28 rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2), Wilcox (US PG Publication 2003/0061458 A1) and Manowitz (US PG Publication 2001/0039603 A1) as applied to claim 26 above, and in further view of Williams (US Patent 6,507,530 B1).

As for claims 27-28, though Nizar fails to teach the second unit of data as a memory module information file. Williams however teaches a weighted throttling mechanism with rank based throttling for a memory system wherein command information (i.e. memory module information file) is obtained from a plurality of device ranks. The controller uses the command information to generate a power weight value based on this information. The controller compares the stored power count of the ranks to a threshold to determine if the controller is to throttle the memory (see abstract). It is worthy to note that power values must be stored while the throttling logic (Fig. 1) increments before the

comparison can be performed (Williams explicitly discloses the use of registers for storage). In other words, a subunit (i.e. power count) is stored to make the determination. Col. 4, lines 4-16 further illustrates storing the power value.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Williams's throttling based mechanism for a memory system in his own memory system. By doing so, Nizar would benefit by having a means of throttling his memory units, hence reducing the likelihood of thermal overstress of the memory, as taught by Williams, col. 1, lines 33-38.

16. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2), Wilcox (US PG Publication 2003/0061458 A1), Manowitz (US PG Publication 2001/0039603 A1), and Williams (US Patent 6,507,530 B1) as applied to claim 28 above, and in further view of Koga (US PG Publication 2001/0026487 A1).

As for claim 29, Nizar fails to teach the information as including the operating frequencies of the memory.

Koga however teaches storing the operating frequencies and manufacturer of the memories in the memories themselves (paragraph 0031, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to include Koga's apparatus into his own memory module system. By doing so, Nizar would benefit by having a memory module system that achieves a higher operation speed by utilizing both on-board type memory modules, and slot-type

memory modules to reduce the need to increase the installation area as taught by Koga (paragraph 0012, all lines).

As for claim 30, Nizar teaches accessing the second unit in response to initial booting of the computer system (Fig. 6 describes the process starting with system restart).

17. Claims 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2), Williams (US Patent 6,507,530 B1), Manowitz (US PG Publication 2001/0039603 A1), Wilcox (US PG Publication 2003/0061458 A1), Koga (US PG Publication 2001/0026487) as applied to claims 5, 17, and 37 above, and in further view Azevedo (US PG Publication 2003/0221072 A1).

As for claim 31, Nizar fails to teach the second unit of data as being accessed in response to a change in the memory controller register.

Azevedo however teaches an apparatus for increasing processor performance in a computing system, which includes a memory controller which contains a dirty bit. The dirty bit indicates if data in the memory has been changed. If the dirty bit is changed to indicate the line is dirty, the controller will access the memory by flushing the cache (paragraph 0065, all lines). In other words, once a change occurs to this bit (i.e. register), the memory will be accessed.

As for claim 32, again Nizar fails to teach the second unit of data as being accessed in response to an indication that the module information file have not be accessed.

Azevedo however teaches requesting data depending on the validity of the data and the tag portion of the address. The memory can be accessed if it is determined that an exact comparison occurs (data is valid as it has not been accessed since newly written – paragraph 0061, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Azevedo's apparatus into his own memory system. By doing so, Nizar could improve his processor's response to memory requests as suggested by Azevedo in paragraph 0020, all lines.

18. Claim 13 is rejected under 35 U.S.C. 103(a) by Nizar et al. (US Patent 6,378,056 B2), hereinafter Nizar in further view of Wilcox (US PG Publication 2003/0061458 A1).

As for claim 13, Nizar teaches a method, system and machine-readable medium comprising:

a memory unit (Fig. 1, element 104); and

a first unit (Fig. 5, element 500 – memory controller, or MCH) to access a first unit of data from a Serial Presence Detect (SPD) device of the memory unit (referring to Fig. 5, and col. 13, line 52 through col. 14, line 8 – information stored in the module's SPD is read by the MCH via the serial interface in the ICH (element 505)), and the first unit to access, via the first unit of data, a second unit of data stored separately from the first unit of data (col. 14, lines 26-37 – SPD configuration data is read from the RDRAM devices. The memory controller registers are then programmed with values from the SPD so that each RDRAM device can be uniquely accessed by the controller – Also, please note in Fig. 5,

element 572 – the module's SPD are at a different location than the RDRAMs). In other words, the data (i.e. a second unit of data) in the RDRAMs can be accessed once the controller is programmed with values extracted from the SPD (i.e. via the first unit of data).

Though Nizar teaches all of the previously described elements of claim 13, he fails to teach his system including a cd-rom drive as recited in claim 25.

Wilcox however teaches a memory control with lookahead power management system, which includes a his system as utilizing a cd-rom drive (paragraph 0022, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Wilcox's system of power management. By doing so, Nizar could benefit by further including a means of reducing power consumption of DRAM devices, by placing them into low power states while not in use, as taught by Wilcox (paragraph 0003 – all lines).

19. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2) and Wilcox (US PG Publication 2003/0061458 A1) as applied to claim 13 above, and in further view of Manowitz (US PG Publication 2001/0039603 A1).

As for claim 14, though Nizar teaches accessing a second unit of data, he fails to teach accessing one from a group comprising a hard disk, floppy disk, CD-ROM or a separate computer interconnected via a network.

Manowitz however teaches a system which stores solid state memory cards in a device bay over a network (referring to Fig. 3 – element 212). It is worthy to note that the bay it self is just one of a plurality of elements including a separate computer (Fig. 2, PC element 206) of the network – (paragraphs 0017 and 0018, all lines). Therefore the device bay (Fig. 2, element 212) can be accessed via the computer through the network.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Manowitz's networked device bay storage for his own to access his own memory modules. By doing so, Nizar would benefit by having a system to dynamically change the memory capacity of his system over a network by simply adding or removing modules from the bay (paragraph 0015, all lines). Nizar would also benefit by using the IEEE-1394 interface, which prevents data loss during live connection/disconnection of the memory (paragraph 0002, all lines).

20. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2), Wilcox (US PG Publication 2003/0061458 A1), and Manowitz (US PG Publication 2001/0039603 A1) as applied to claim 14 above, and in further view of Williams et al. (US Patent 6,507,530 B1), hereinafter Williams.

As for claims 15-16, though the combined teachings of Nizar, Wilcox and Manowitz fail to teach the second unit of data as a memory module information file. Williams however teaches a weighted throttling mechanism with rank based throttling for a memory system wherein command information (i.e. memory

module information file) is obtained from a plurality of device ranks. The controller uses the command information to generate a power weight value based on this information. The controller compares the stored power count of the ranks to a threshold to determine if the controller is to throttle the memory (see abstract). It is worthy to note that power values must be stored while the throttling logic (Fig. 1) increments before the comparison can be performed (Williams explicitly discloses the use of registers for storage). In other words, a subunit (i.e. power count) is stored to make the determination. Col. 4, lines 4-16 further illustrates storing the power value.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Williams's throttling based mechanism for a memory system in his own memory system. By doing so, Nizar would benefit by having a means of throttling his memory units, hence reducing the likelihood of thermal overstress of the memory, as taught by Williams, col. 1, lines 33-38.

21. Claims 17-18, 21 and 23, are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2), Wilcox (US PG Publication 2003/0061458 A1), and Manowitz (US PG Publication 2001/0039603 A1) and Williams (US Patent 6,507,530 B1) as applied to claims 4, 16 and 36 above, and in further view Koga (US PG Publication 2001/0026487 A1).

As for claim 17, the combined teachings of Nizar, Wilcox, Manowitz, and Williams fail to teach the information stored in his memory modules as including the either operating frequencies, or the manufacturer of the memories.

Koga however teaches storing the operating frequencies and manufacturer of the memories in the memories themselves (paragraph 0031, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to include Koga's apparatus into his own memory module system. By doing so, Nizar would benefit by having a memory module system that achieves a higher operation speed by utilizing both on-board type memory modules, and slot-type memory modules to reduce the need to increase the installation area as taught by Koga (paragraph 0012, all lines).

As for claim 18, Nizar teaches accessing the second unit in response to initial booting of the computer system (Fig. 6 describes the process starting with system restart).

As for claim 21, Nizar teaches the information as being accessed by the BIOS (col. 3, lines 58-67).

As for claim 23, Koga teaches the information as including the manufacturer and operating frequencies of the memory (described in the rejection of claim 5 above).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to include Koga's apparatus into his own memory module system. By doing so, Nizar would benefit by having a memory module system that achieves a higher operation speed by utilizing both on-board type memory modules, and slot-type

memory modules to reduce the need to increase the installation area as taught by Koga (paragraph 0012, all lines).

22. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2), Wilcox (US PG Publication 2003/0061458 A1), Manowitz (US PG Publication 2001/0039603 A1), Williams (US Patent 6,507,530 B1), Koga (US PG Publication 2001/0026487 A1) as applied to claims 5, 17, and 37 above, and in further view Azevedo et al. (US PG Publication 2003/0221072 A1), hereinafter Azevedo.

As for claim 19, Nizar fails to teach the second unit of data as being accessed in response to a change in the memory controller register.

Azevedo however teaches an apparatus for increasing processor performance in a computing system, which includes a memory controller which contains a dirty bit. The dirty bit indicates if data in the memory has been changed. If the dirty bit is changed to indicate the line is dirty, the controller will access the memory by flushing the cache (paragraph 0065, all lines). In other words, once a change occurs to this bit (i.e. register), the memory will be accessed.

As for claim 20, again Nizar fails to teach the second unit of data as being accessed in response to an indication that the module information file have not be accessed.

Azevedo however teaches requesting data depending on the validity of the data and the tag portion of the address. The memory can be accessed if it is determined that

an exact comparison occurs (data is valid as it has not been accessed since newly written – paragraph 0061, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include Azevedo's apparatus into his own memory system. By doing so, Nizar could improve his processor's response to memory requests as suggested by Azevedo in paragraph 0020, all lines.

23. Claim 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nizar (US Patent 6,378,056 B2), Wilcox (US PG Publication 2003/0061458 A1), Manowitz (US PG Publication 2001/0039603 A1), Williams (US Patent 6,507,530 B1), Koga (US PG Publication 2001/0026487 A1) as applied to claims 10 and 21 above, and in further view Haas et al. (US PG Publication 2005/0050266 A1), hereinafter Haas.

As for claim 22 Nizar fails to teach parsing the information file as recited in these claims.

Haas however teaches a method for storing data independent memories, which includes parsing data into data segments, and storing those segments into a non-volatile memory (paragraph 0020, lines 1-10). Examples of non-volatile memory are provided in paragraph 0029, lines 1-13.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nizar to further include parsing of the data into his own memory system. By doing so, Nizar would have a means of providing redundancy for data in his system, in case a memory failure occurs as taught by Haas (paragraph 0002, all lines).

24. As for claim 24, though Williams teaches his information file as supporting DRAM, he fails to teach support SRAM, or FLASH memory. However it would have been obvious to a person of ordinary skill in the art at the time of the invention to further include these two well known memories. One of ordinary skill in the art would have been motivated to do so, to improve the access time to the memory.

Examiner takes Official Notice (see MPEP section 2144.03) that these two memories were well known when the invention was made. The Applicant is entitled to traverse any/all official notice taken in this action according to MPEP section 2144.03. However, MPEP section 2144.03 further states "See also In re Boon, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice)." Specifically, In re Boon, 169 USPQ 231, 234 states "as we held in Ahlert, an applicant must be given the opportunity to challenge either the correctness of the fact asserted or the notoriety or repute of the reference cited in support of the assertion. We did not mean to imply by this statement that a bald challenge, with nothing more, would be all that was needed". Further note that 37 CFR section 671(c)(3) states "Judicial notice means official notice". Thus, a traversal by the Applicant that is merely "a bald challenge, with nothing more" will be given very little weight.

Since Applicant has failed to traverse Examiner's assertion that SRAM and FLASH memories are well-known in art in response to the previous correspondence, these memories are taken to be admitted prior-art per MPEP § 2144.03 (paragraph C).

Response to Arguments

25. Examiner's response to Applicant's remarks are presented below:

Applicant asserts that claims 1, 7, 10, 13, 19, 22, 25, 26, 31, 33, 39, 42 have been amended, however Examiner believes that claims 1, 7, 10-**11**, 13-**14**, 19, 22-**23**, 25, 26, 31, 33, 39, 42 have been amended.

Applicant has declined to comply with Examiner's request for a brief summary by citing appropriate sections of the MPEP indicating that this is merely a suggestion for, and not a requirement of Applicant. Examiner agrees with Applicant and respectfully withdrawals the objection. Though the objection is withdrawn, Examiner would like to make a final attempt to encourage Applicant to provide Examiner with a brief summary. Said summary would greatly facilitate a search of the prior art should the instant application mature to a patent.

Applicant asserts that the alleged misspelled words in the specification (i.e. field and drawings) were caused by a scanning error rather than a deficiency in the actual document. Examiner agrees and respectfully withdrawals these objections.

Examiner maintains the objection to Figure 3 per the discussion *supra* (paragraph heading 4).

26. Applicant's arguments with respect to rejection of the claims have been fully considered but are not persuasive:

Applicant's arguments with respect to claim 33-42 (under 35 USC §101) have been fully considered but are not persuasive. Referring to Annex IV of the Interim Guidelines for Examination of Patent Application for Patent Subject Matter Eligibility, claims to signals and carrier waves are not held to be patentable subject matter. Therefore, the rejection of these claims is maintained. Said guidelines may be accessed via the web at: http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf

Applicant's arguments with respect to claim 1, 13, 33 (under 35 USC §102) have been fully considered but are not persuasive.

As for claim 1, 13 and 33, Applicant asserts that Nizar fails to teach "the first unit of data including characteristics of the memory unit". Likewise, Applicant asserts that Nizar fails to teach, "accessing, based on content of the first unit of data, a second unit of data stored in a separate storage device from the memory unit to retrieve additional characteristics of the memory unit". Applicant contrasts these limitations with Nizar by alleging that Nizar merely teaches configuring the RDRAM devices based on the contents of the SPD in the memory unit. Applicant additionally assets that Nizar fails to teach storing characteristic data elsewhere. Examiner however maintains that Nizar in fact does teach accessing a second unit of data based on the first data to retrieve additional characteristics of the of the memory, and that said first data itself contains

characteristics of the memory unit. More specifically, col. 14, lines 26-37 describe the SPD configuration data as being read from the RDRAM devices. The memory controller registers are then programmed with values from the SPD so that the controller can uniquely access each RDRAM device. Referring to Fig 5, the memory controller (500) comprises initialization registers (515) used to store information related to each of the RDRAM device (col. 13, lines 21-43). Once the initialization process begins, data related to the RDRAMs is read from the SPD. This information is then used to populate the controller's registers (i.e. separate storage device) with characteristic data on each RDRAM (col. 14, lines 26-37). The system must now use the information in the controller's registers in order to appropriately access the RDRAM devices (col. 14, lines 38-52). In summary, the system accesses the SPD in order to obtain configuration data, which in turn is used to program registers of the memory controller. Once the system is initialized, the characteristic data must be accessed from the controller registers in order to extract the appropriate information to access the RDRAM devices. The registers of the controller are separate from the SPD non-volatile memory location.

Applicant's arguments with respect to claim 2-12, 14-32, and 34-42 (under 35 USC §103) have been fully considered but are not persuasive.

As for claim 25, the same justification for maintaining the rejection of clam 1 applies to this claim.

As for claims 2-12, 14-24, 26-32, and 34-42, the argument that these claims are allowable for depending upon allowable independent claims 1, 15, 25, and 33 is rendered moot as the Examiner maintains the original rejections to these independent claims, with changes as needed to address the amendments.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

28. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

Mano Padmanabhan
7/5/06

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